



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. .... 10/803,264  
Filing Date ..... March 17, 2004  
Inventor..... Warren M. Farnworth et al.  
Assignee ..... Micron Technology, Inc.  
Group Art Unit.....2829  
Examiner ..... Russell Marc Kobert  
Attorney's Docket No. ....MI22-2524  
Title: Method and Apparatus for Testing Semiconductor Circuitry for Operability and  
Method of Forming Apparatus for Testing Semiconductor Circuitry for Operability

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**


Reference - - See attached Form PTO-1449

The attached Form PTO-1449 is submitted in compliance with 37 C.F.R. §§ 1.56.  
Pursuant to Federal Register Vol. 69, No. 182, pg. 56542 (September 21, 2004), no copies  
of any cited U.S. patents or U.S. published applications are included herewith. No  
admission is made regarding whether the submitted reference is prior art.

Citation of this reference is respectfully requested.

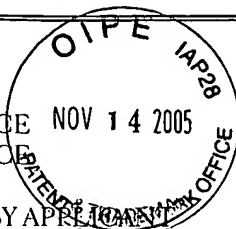
Respectfully submitted,

Date: 11-14-05

  
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MI22-2524SERIAL NO.  
10/803,264APPLICANT  
Warren M. Farnworth et al.FILING DATE  
March 17, 2004GROUP  
2829

## U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,686,758	02/04	Farnworth et al.	324	765	
	AB	5,201,992	04/93	Marcus	216	11	
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
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	AJ						

## FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AK							
	AL							
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## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.